## What is claimed is:

[Claim 1] 1. A method of measuring capacitance, comprising:

providing a first switch, wherein a terminal of the first switch is connected to a terminal of a first capacitor;

providing a second switch, wherein a terminal of the second switch is connected to a terminal of a second capacitor;

providing a third switch, wherein a terminal of the third switch is connected to another terminal of the first capacitor and another terminal of the second capacitor; and

providing a P-type transistor, wherein a gate of the P-type transistor is connected to another terminal of the third switch;

wherein when the first switch, the second switch and the third switch are turned on, a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance of first capacitor and the capacitance of the second capacitor is measured via the another terminal of the first switch, the another terminal of the second switch, and a source and a drain of the P-type transistor.

[Claim 2] 2. A circuit for measuring capacitance, comprising:

a first switch, wherein a terminal of the first switch is connected to a terminal of a first capacitor;

a second switch, wherein a terminal of the second switch is connected to a terminal of a second capacitor;

a third switch, wherein a terminal of the third switch is connected to another terminal of the first capacitor and another terminal of the second capacitor; and

a P-type transistor, wherein a gate of the P-type transistor is connected to another terminal of the third switch;

wherein when the first switch, the second switch and the third switch are turned on, a capacitance of the first capacitor, a capacitance of the second capacitor, or a ratio of a difference between the capacitance of first capacitor and the capacitance of the second capacitor to an average of the capacitance

of first capacitor and the capacitance of the second capacitor is measured via the another terminal of the first switch, the another terminal of the second switch, and a source and a drain of the P-type transistor.

[Claim 3] 3. A method of measuring at least two capacitor pairs, wherein each of the capacitor pairs comprises at least a first capacitor and a second capacitor, the method comprising:

providing a first switch to each of the capacitor pair respectively, wherein a terminal of each of the first switch is connected to a terminal of the first capacitor of the corresponding capacitor pair, and another terminal of each of the first switch is connected to a first pad respectively;

providing a second switch to each of the capacitor pair respectively, wherein a terminal of each of the second switch is connected to a terminal of the second capacitor of the corresponding capacitor pair, and another terminal of each of the second switch is connected to a second pad respectively;

providing a third switch to each of the capacitor pair respectively, wherein a terminal of each of the third switch is connected to another terminal of the first capacitor and another terminal of the second capacitor of the corresponding capacitor pair; and

providing a P-type transistor, wherein a gate of the P-type transistor is connected to another terminal of the third switch of all of the capacitor pairs;

wherein a capacitance of one of the first capacitors, a capacitance of one of the second capacitors, or a ratio of a difference between the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors to an average of the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors is measured via the first pad, the second pad, and a source and a drain of the P-type transistor.

[Claim 4] 4. The method of claim 3, wherein when the first switch, the second switch and the third switch of one of the capacitor pair are turned on, for the one of the capacitor pair, the capacitance of the first capacitor thereof, the capacitance of the second capacitor thereof, or a ratio of a difference between the capacitance of the first capacitor and the capacitance of the second capacitor to an

average of the capacitance of the first capacitor and the capacitance of the second capacitor thereof is measured.

[Claim 5] 5. The method of claim 3, wherein when the first switch and the third switch of one of the capacitor pair, and the second switch and the third switch of another one of the capacitor pair are turned on, the capacitance of the first capacitor of the one of the capacitor pair, the capacitance of the second capacitor of the another one of the capacitor pair, or a ratio of a difference between the capacitance of the first capacitor of the one of the capacitor pair and the capacitance of the second capacitor of the another one of the capacitor pair to an average of the capacitance of the first capacitor of the one of the capacitor pair and the capacitance of the second capacitor of the another one of the capacitor pair is measured.

[Claim 6] 6. The method of claim 3, further comprising:

providing a selection circuit, connected to all of the first switches, the second switches and the third switches to selectively turn on or turn off the first switches, the second switches or the third switches.

[Claim 7] 7. The method of claim 6, further comprising a step of automatically operating the method via the selection circuit.

[Claim 8] 8. The method of claim 6, wherein the selection circuit comprises a shift register.

[Claim 9] 9. A circuit for measuring at least two capacitor pairs, wherein each of the capacitor pairs comprises at least a first capacitor and a second capacitor, the circuit comprising:

a plurality of first switches, wherein a terminal of each of the first switch is connected to a terminal of the first capacitor of each of the capacitor pairs, and another terminal of all of the first switch is connected to a first pad;

a plurality of second switches, wherein a terminal of each of the second switch is connected to a terminal of the second capacitor of each of the capacitor pairs, and another terminal of all of the second switch is connected to a second pad;

a plurality of third switches, wherein a terminal of each of the third switch is connected to another terminal of the first capacitor and another terminal of the second capacitor of each of the capacitor pairs; and

a P-type transistor, wherein a gate of the P-type transistor is connected to another terminal of the third switch of all of the capacitor pairs;

wherein a capacitance of one of the first capacitors, a capacitance of one of the second capacitors, or a ratio of a difference between the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors to an average of the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors is measured via the first pad, the second pad, and a source and a drain of the P-type transistor.

[Claim 10] 10. The circuit of claim 9, wherein when the first switch, the second switch and the third switch of one of the capacitor pair are turned on, for the one of the capacitor pair, the capacitance of the first capacitor thereof, the capacitance of the second capacitorthereof, or a ratio of a difference between the capacitance of the first capacitor and the capacitance of the second capacitor to an average of the capacitance of the first capacitor and the capacitance of the second capacitor thereof is measured.

[Claim 11] 11. The circuit of claim 9, wherein when the first switch and the third switch of one of the capacitor pair, and the second switch and the third switch of another one of the capacitor pair are turned on, the capacitance of the first capacitor of the one of the capacitor pair, the capacitance of the second capacitor of the another one of the capacitor pair, or a ratio of a difference between the capacitance of the first capacitor of the one of the capacitor pair and the capacitance of the second capacitor of the another one of the capacitor pair to an average of the capacitance of the first capacitor of the one of the capacitor pair and the capacitance of the second capacitor of the another one of the capacitor pair is measured.

[Claim 12] 12. The circuit of claim 9, further comprising:

a selection circuit, connected to all of the first switches, the second switches and the third switch to selectively turn on or turn off the first switches, the second switches or the third switches.

[Claim 13] 13. The circuit of claim 12, further comprising a step of automatically operating the circuit via the selection circuit.

[Claim 14] 14. The circuit of claim 12, the selection circuit comprises a shift register.